UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,749	11/26/2001	Yoh Takano	011503	5326

38834 7590 08/26/2004

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
DANIEL JR, WILLIE J	

ART UNIT	PAPER NUMBER
2686	6

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/991,749	TAKANO ET AL.	
	Examiner	Art Unit	
	Willie J. Daniel, Jr.	2686	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 February 2002 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because Fig. 1 includes components that lack reference numbers and not spoken of in the description which are the following:

   a. The component shares a node on the right end with component 28 and on the left end with components 20 and 21.

   b. The component shares a node with component 22 on the top end and ground on the bottom end.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

a. Fig. 3 does not include "ref. 220" as stated on pg. 16, 1st paragraph, line 6.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muschallik et al. (hereinafter Muschallik) (US 6,636,727 B2) in view of Shiga et al. (hereinafter Shiga) (US 6,240,019 B1).

Regarding **Claim 1**, Muschallik discloses an electronic tuning system (see abstract; col. 5, lines 13-33; Fig. 1), where the system is for tuning of received system comprising:

a voltage controlled oscillator (29, 45) for generating a local frequency signal having a frequency according to a tuning voltage which reads on the claimed "predetermined control voltage" (see col. 5, lines 56-63; col. 6, lines 6-8; col. 7, line 61 - col. 8, line 2; Fig. 1);

a channel selection device (75) which reads on the claimed "electronic tuner" coupled to the voltage controlled oscillator (45) for adjusting the predetermined control voltage to tune the local frequency signal to radio waves on an arbitrary channel in accordance with channel selection information (see col. 7, lines 13-26; Fig. 1);

a charge pump (88) which reads on the claimed "booster circuit" coupled to the voltage controlled oscillator (45) for boosting a source voltage to generate a boosted voltage in order to ensure the predetermined control voltage (see col. 7, line 51 - col. 8, line 2), where the source voltage would be obvious; and

a memory device (73) which reads on the claimed memory for storing the channel selection information (see col. 7, lines 13-26; col. 10, lines 12-37).

Muschallik fails to disclose having the features of a non-volatile memory; in response to a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the feature of a non-volatile memory; in response to a predetermined write voltage wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage was well known in the art, as taught by Shiga.

In the same field of endeavor, Shiga discloses the feature of a memory cell array (1) which reads on the claimed "non-volatile memory" (see col. 3, lines 12-15; col. 5, lines 30-35; Fig. 1), where the memory is a flash memory;

in response to a predetermined write voltage wherein the boosted voltage of the booster circuit (7) is utilized as the predetermined write voltage (see abstract; col. 6, lines 23-40; Fig. 5), where the data is stored according to write voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Muschallik and Shiga to have the features of a non-volatile memory; in response to a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage, in order to store data in accordance to a boosted write voltage, as taught by Shiga.

Regarding **Claim 2**, the combination of Muschallik and Shiga discloses every limitation claimed, as applied above (see claim 1), in addition Muschallik further discloses the electronic tuning system according to claim 1, wherein the electronic tuner includes:

a frequency divider (71) coupled to the voltage controlled oscillator (45) for dividing the oscillator frequency which reads on the claimed "local frequency signal" in accordance with a predetermined frequency division ratio to generate a divided local frequency signal (see col. 7, lines 6-11,33-38; Fig. 1);

a phase comparator (83) coupled to the frequency divider (71) for comparing the frequency and phase of the divided local frequency signal with the frequency and phase of a reference frequency signal to generate a voltage signal proportional to the frequency difference and the phase difference (see col. 7, lines 33-38,48-51; Fig. 1); and

a loop filter (92) which reads on the claimed "low-pass filter" coupled to the phase comparator (83) for filtering a voltage signal to generate a filtered voltage signal, wherein the predetermined control voltage is generated by adding the boosted voltage to the voltage of the filtered voltage signal, and the channel selection information includes information on the predetermined frequency division ratio supplied to the frequency divider (see col. 7, line 52 - col. 8, line 2; col. 8, lines 11-24; col. 10, lines 12-36; Fig. 1).

Regarding **Claim 3**, the combination of Muschallik and Shiga discloses every limitation claimed, as applied above (see claim 2), in addition Muschallik further discloses the electronic tuning system according to claim 2, wherein the voltage controlled oscillator includes:

a varactor diode (32) which varies its capacitance in response to the predetermined control voltage (see col. 7, lines 61-66; Fig. 1); and

a local oscillator (29) coupled to the varactor diode (32) for generating a local frequency signal having a frequency in accordance with the capacitance of the varactor diode (32) (see col. 5, lines 56-64; Fig. 1).

Regarding **Claim 5**, Muschallik fails to disclose having the feature of a voltage supply control circuit coupled to the booster circuit for supplying the boosted voltage to the non-volatile memory in response to a request for writing the channel selection information into the non-volatile memory. However, the examiner maintains that the feature a voltage supply control circuit coupled to the booster circuit for supplying the boosted voltage to the non-volatile memory in response to a request for writing the channel selection information into the non-volatile memory was well known in the art, as taught by Shiga.

Shiga further discloses feature a power supply control system (7) which reads on the claimed "voltage supply control circuit" coupled to the booster circuit (7) for supplying the boosted voltage to the non-volatile memory (1) in response to a request for writing the data which reads on the claimed "channel selection information" into the non-volatile memory (1) (see abstract; col. 3, lines 12-15; col. 6, lines 23-40; Figs. 5, 27, 29A-B), where the booster circuit provides power supply control of the boosted voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Muschallik and Shiga to have the feature a voltage supply control circuit coupled to the booster circuit for supplying the boosted voltage to the non-volatile memory in response to a request for writing the channel selection information into the non-volatile memory, in order to store data in accordance to a boosted write voltage, as taught by Shiga.

Regarding **Claim 6**, Muschallik fails to disclose having the feature wherein the non-volatile memory includes a flash memory which receives the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage. However, the examiner maintains that the feature wherein the non-volatile memory includes a flash memory which receives the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage was well known in the art, as taught by Shiga.

Shiga further discloses the feature wherein the non-volatile memory (1) includes a flash memory (1) which receives the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage (see abstract; col. 3, lines 12-15; col. 5, lines 30-35; col. 6, lines 23-40; Figs. 5, 9, 26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Muschallik and Shiga to have the feature wherein the non-volatile memory includes a flash memory which receives the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage, in order to read, write, or erase data in accordance to a booster circuit voltage, as taught by Shiga.

Regarding **Claim 7**, Muschallik fails to disclose having the feature wherein the non-volatile memory includes a voltage converter circuit coupled to the booster circuit for receiving the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage. However, the examiner maintains that the feature wherein the non-volatile memory includes a voltage converter circuit coupled to the booster circuit for receiving the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage was well known in the art, as taught by Shiga.

Shiga further discloses the feature wherein the non-volatile memory (1) includes a regulator (8) which reads on the claimed "voltage converter circuit" coupled to the booster circuit (7) for receiving the boosted voltage from the booster circuit (7) to generate an erasure voltage and a write voltage (see abstract; col. 3, lines 12-15; col. 5, lines 30-35; col. 6, lines 23-40; Figs. 5, 9, 26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Muschallik and Shiga to have the feature wherein the non-volatile memory includes a voltage converter circuit coupled to the booster circuit for receiving the boosted voltage from the booster circuit to generate an erasure voltage and a write voltage, in order to read, write, or erase data in accordance to a booster circuit voltage, as taught by Shiga.

Regarding **Claim 8**, Muschallik fails to disclose having the feature further comprising a voltage supply control circuit coupled between the booster circuit and the voltage converter circuit for supplying the boosted voltage to the voltage converter circuit in response to a request for writing the channel selection information into the non-volatile memory. However, the examiner maintains that the feature further comprising a voltage supply control circuit coupled between the booster circuit and the voltage converter circuit for supplying the boosted voltage to the voltage converter circuit in response to a request for writing the channel selection information into the non-volatile memory was well known in the art, as taught by Shiga.

Shiga further discloses the feature further comprising a voltage supply control circuit (7) coupled between the booster circuit (7) and the voltage converter circuit (8) for supplying

the boosted voltage to the voltage converter circuit (8) in response to a request for writing the data which reads on the claimed "channel selection information" into the non-volatile memory (1) (see abstract; col. 3, lines 12-15; col. 5, lines 30-35; col. 6, lines 23-40; Figs. 5, 9, 26, 27, 29A-B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Muschallik and Shiga to have the feature further comprising a voltage supply control circuit coupled between the booster circuit and the voltage converter circuit for supplying the boosted voltage to the voltage converter circuit in response to a request for writing the channel selection information into the non-volatile memory, in order to read, write, or erase data in accordance to a booster circuit voltage, as taught by Shiga.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muschallik et al. (hereinafter Muschallik) (US 6,636,727 B2) in view of Shiga et al. (hereinafter Shiga) (US 6,240,019 B1) as applied to claim 1 above, and further in view of Ogita (US 4,225,823).

Regarding **Claim 4**, the combination of Muschallik and Shiga fails to disclose the feature wherein the booster circuit includes: a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage. However, the

examiner maintains that the feature wherein the booster circuit includes: a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage was well known in the art, as taught by Ogita.

In the same field of endeavor, Ogita discloses the feature wherein the booster amplifier (79) which reads on the claimed "booster circuit" (see col. 6, lines 3-31; Fig. 5) includes:

a coil (76) coupled to a voltage source (+B) which reads on the claimed "power source" (see col. 6, lines 12-15; Fig. 5);

a switching element (81) coupled to the coil (76) for periodically conducting a DC current flowing through the coil to a ground to change the DC current (see col. 6, lines 12-18; Fig. 5);

a zener diode (89) coupled to the coil (76) for clamping an electromotive force induced in the coil (76) in accordance with a change in the DC current flowing through the coil (76) to a predetermined voltage (see col. 6, lines 12-31; Fig. 5), where the clamping of the EMF would be obvious; and

a capacitor (77) coupled to the zener diode (89) for smoothing the clamped voltage to generate a boosted voltage (see col. 6, lines 24-31; Fig. 5), where the signal flows through the capacitor in which smoothing of the voltage would be obvious.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Muschallik and Shiga with Ogita to have the feature wherein the booster circuit includes: a coil coupled to a power source; a switching element coupled to the coil for periodically conducting a DC current flowing through the coil to a ground to change the DC current; a zener diode coupled to the coil for clamping an electromotive force induced in the coil in accordance with a change in the DC current flowing through the coil to a predetermined voltage; and a capacitor coupled to the zener diode for smoothing the clamped voltage to generate a boosted voltage, in order to boost the power of the signal, as taught by Ogita.

Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muschallik et al. (hereinafter Muschallik) (US 6,636,727 B2) in view of Yanagibori (US 4,919,640) and Shiga et al. (hereinafter Shiga) (US 6,240,019 B1).

Regarding **Claim 9**, Muschallik discloses a broadcast receiver which reads on the claimed "radio receiver" (see col. 5, lines 19-21; Fig. 1) comprising:

a voltage controlled oscillator (29) for generating a local frequency signal having a frequency in accordance with a predetermined control voltage (tuning voltage) (see col. 5, lines 56-63; col. 6, lines 6-8; col. 7, line 61 - col. 8, line 2; Fig. 1);

a mixing device (27, 39) which reads on the claimed "mixer" coupled to the voltage controlled oscillator (29, 45) for mixing a received signal with a local frequency signal to generate a mixed frequency signal (see col. 6, lines 36-41; Fig. 1);

an bandpass filter (20) which reads on the claimed "intermediate frequency filter" coupled to the mixer (27) for filtering the mixed frequency signal to generate an intermediate frequency signal (see col. 5, lines 45-54; col. 5, line 64 - col. 6, line 3; col. 6, line 36-44; Fig. 1);

an electronic tuner (75) coupled to the voltage controlled oscillator (45) for adjusting the predetermined control voltage to tune the local frequency signal to radio waves on an arbitrary channel in accordance with channel selection information (see col. 7, lines 13-26; Fig. 1);

a booster circuit (88) coupled to the voltage controlled oscillator (45) for boosting a source voltage to generate a boosted voltage in order to ensure a predetermined control voltage (see col. 7, line 51 - col. 8, line 2), where the source voltage would be obvious. Also, Muschallik discloses of a memory device (73) which reads on the claimed memory for storing the channel selection information (see col. 7, lines 13-26; col. 10, lines 12-37). Muschallik fails to disclose having the features a detector circuit coupled to the intermediate frequency filter for demodulating the intermediate frequency signal to an audio signal; a non-volatile memory for storing the channel selection information in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the feature of a detector circuit coupled to the intermediate frequency filter for demodulating the intermediate frequency signal to an audio signal was well known in the art, as taught by Yanagibori.

In the same field of endeavor, Yanagibori discloses the feature of a detector circuit (16) coupled to the intermediate frequency filter (15) for demodulating the intermediate frequency signal to an audio signal (see col. 4, lines 2-10; Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Muschallik and Yanagibori to have the feature of a detector circuit coupled to the intermediate frequency filter for demodulating the intermediate frequency signal to an audio signal, in order to supply the detected output to, for example, a power amplifier to loudspeaker, as taught by Yanagibori. The combination of Muschallik and Yanagibori fails to disclose having the feature a non-volatile memory for storing the channel selection information in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage. However, the examiner maintains that the feature a non-volatile memory for storing the channel selection information in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage was well known in the art, as taught by Shiga.

Shiga further discloses the feature a non-volatile memory (1) for storing the channel selection information (data) in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit (7) is utilized as the predetermined write voltage (see abstract; col. 3, lines 12-15; col. 5, lines 30-35; col. 6, lines 23-40; Figs. 5, 9, 26), where the data is stored according to write voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Muschallik and Yanagibori with Shiga

to have the feature a non-volatile memory for storing the channel selection information in accordance with a predetermined write voltage, wherein the boosted voltage of the booster circuit is utilized as the predetermined write voltage, in order to store data in accordance to a boosted write voltage, as taught by Shiga.

Regarding **Claim 10**, the combination of Muschallik, Yanagibori, and Shiga discloses every limitation claimed, as applied above (see claim 9), in addition Muschallik further discloses the radio receiver according to claim 9, wherein the electronic tuner (see abstract; col. 5, lines 19-21; Fig. 1) includes:

a frequency divider (71) coupled to the voltage controlled oscillator (45) for dividing the oscillator frequency which reads on the claimed "local frequency signal" in accordance with a predetermined frequency division ratio to generate a divided local frequency signal (see col. 7, lines 6-11,33-38; Fig. 1);

a phase comparator (83) coupled to the frequency divider (71) for comparing the frequency and phase of the divided local frequency signal with the frequency and phase of a reference frequency signal to generate a voltage signal proportional to the frequency difference and the phase difference (see col. 7, lines 33-38,48-51; Fig. 1); and

a loop filter (92) which reads on the claimed "low-pass filter" coupled to the phase comparator (83) for filtering a voltage signal to generate a filtered voltage signal, wherein the predetermined control voltage is generated by adding the boosted voltage to the voltage of the filtered voltage signal, and the channel selection information includes information on the predetermined frequency division ratio supplied to the frequency divider (see col. 7, line 52 - col. 8, line 2; col. 8, lines 11-24; col. 10, lines 12-36; Fig. 1).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. Higuchi (US 5,881,364) discloses "Radio Pager Having Correcting Circuit Responsive To Temperature Variation".

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Willie J. Daniel, Jr. whose telephone number is (703) 305-8636. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on (703) 305-4379. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WJD,JR
12 August 2004

8/20/04
LESTER G. KINCAID
PRIMARY EXAMINER